ABSTRACT

A fail repair circuit in semiconductor memory devices is disclosed. The fail repair circuit can be applied to semiconductor memory devices for receiving a row address and a column address at a time without receiving them divisionally, and semiconductor memory devices operating as a single read mode and a single write mode with no burst or a page mode without address multiplexing. The repair circuit comprises a bit fail repair block for using the column and row addresses to determine whether they are fail addresses in order to decide whether bit repair for the fail addresses are to be performed, a row repair block for determining whether the row addresses are fail and deciding whether row repair for the row addresses are to be performed depending on the output of the bit fail repair block, and a plurality of column repair blocks for deciding whether column repair for the column addresses are to be performed and deciding whether a normal column driver must be selected, depending on the column address, column fuse boxes and an output signal of the bit fail repair block.